CIRCUITRY FOR SYNTHESIZING AN ARBITRARY CLOCK SIGNAL AND METHODS FOR THE SYNTHESIS THEREOF

Abstract of the Disclosure

Circuitry for synthesizing an arbitrary clock signal with minimal jitter is provided. The circuitry of this invention selectively multiplexes a sequence of two different byte patterns into a serializer, which serializes the sequence and transmits it to receiver circuitry in the serial domain. The frequency of the synthesized clock transmitted by the serializer is a function of the serialized sequence and the frequency in which the serialized sequence is transmitted to the receiver circuitry. Thus, a desired clock frequency can be synthesized by manipulating the byte patterns and the sequence in which the bytes are serialized.